Intel® 440MX Entry-level Communications Appliance Reference Design

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5000 W. Chandler Blvd.
Chandler, AZ 85226

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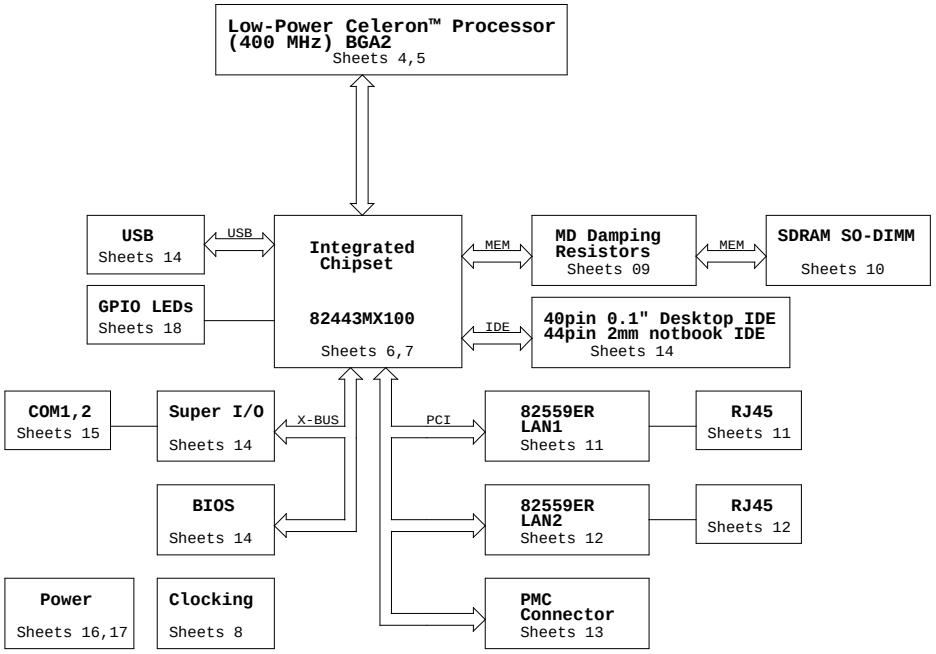
Intel® 440MX Entry-level Communications Appliance Reference Design

Block Diagram



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Title	Block Diagram	
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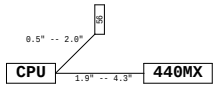
General Board Design Requirements

>> PWB must be routed using six (6) layers, with the following stackup:

Layer 1: Signal, V1P5, V2P5, and V5P0 Busses
Layer 2: Signal, No CPU/BX Traces
Layer 3: Split Power Plane -- V3P3 Plane, V2P0 Island
Layer 4: GND
Layer 5: Signal
Layer 6: Signal

>> Right angle traces must not be used.
>> Vias for decoupling capacitors must be kept as close as possible to the capacitor pad.
>> Trace impedance must be 65 ohms, +/- 10%
>> Total board thickness must be .062".
>> Board material must be FR-4.
>> GND layers must not be split.
>> Top and bottom (outer) layers must be no less than 1/2 oz copper before plating, inner layers must be 1 oz copper.
>> Series terminating resistors must be kept as close to the driving pin as possible.
>> Daisy chain signals going to more that on point, do not use stubs.
>> Unless otherwise noted, all signal traces must be between 5 and 6 mil width.
>> Unless otherwise noted, minimum space between traces is 15 mils, including adjacent layers.
>> Specific routing reqirements are included throughout schematic sheets.
>> One registration target must be included on each corner of the board.

CPU Routing Requirements



>> Route all GTL traces between CPU and 440MX as shown in the diagram to the right.
>> Route all traces between CPU and 440MX on a layer adjacent to a ground plane (preferably bottom layer), without layer changes.
>> All traces between CPU and 440MX should differ in length by no more than 1000 mils.
>> Minimum space between traces is 15 mils (unless otherwise noted), this includes adjacent signal layers.
>> Minimum space between traces may be reduced to 5 mils when breaking out of a footprint. The total length of trace routed using 5 mil spacing must be less than 250 mils.
>> The following signals require 25 mil spacing from other traces, including adjacent layers.

HA#[31:3], HD#[63:0], BREQ0#, ADS#, BNR#, BPRI#, HLOCK#, DEFER#, HTRDY#, DBSY#, DRDY#, HIT#, HITM#, H_A20M#, FLUSH#, H_IGNNE#, H_INIT#, H_INTR, H_NMI, PWR_OK_2P5, PX4_SMI#, SLP#, STPCLK#, 100/66#, FERR#, HRESET#, HREQ#[4:0], RS#[2:0], THERMD[P:N], CPU_GTL_REF[7:0], PLL[2:1], (TCK,TMS,TDI, TDO, TRST#, PRDY#, PREQ#).

>> Route THRMDP and THRMDN close together as a pair (no more than 250 mil difference in length), on same layer, in parallel, and 25 mils min from any other trace.
>> Route CPU_GTLREF using 25 mil minimum width trace, and separate from all other traces by 25 mils minimum.
>> Route PLL[2:1] using 25 mil minimum width trace, minimize loop area, and separate from all other traces by 25 mils minimum.

Clock Specific Routing Requirements

>> A clock trace must not alternate layers.
>> A clock trace must be separated by a minimum of 25 mils from any other trace, including serpentines, 11 mils is OK when going betwen pins or balls.
>> The CPU clock length must be between 1" and 9", and 460 mils shorter than the 440MX clock. The 440MX clock and all PCI clocks must be matched in length, except for the PMC clock which must be 2" shorter than all other PCI clocks.
>> SDRAM_CLK[1:0] must be matched in length, and between 1" and 3" in length.
>> CLKOUT, from the SDRAM clock driver to the 440MX, must be between 3.5" and 5.5" in length, and 2.5" longer than SDRAM_CLK[1:0].
>> Trace length between BX-DCLK0 and SDRAM clock driver (signal REF) must be between 1" and 6".

IDE Specific Routing Requirements

>> Place IDE conector within 3" of 440MX.
>> Place IDE series terminating resistors within 500 mils of the 440MX.

Power Supply Specific Routing Requirements

>> All unrelated signals and power planes must be kept away from the switching circuits.
>> All traces associated with the input power/ground connectors, and the capacitors connected to these connectors, must be routed with minimum length and maximum width.
>> See the Power Supply schematic sheet for complete restrictions.

Memory Bus Specific Routing Requirements

>> Minimum trace width is 5 mils.
>> Minimum space between traces is 10 mils, this includes adjacent signal layers.
>> Minimum space between memory traces and other types of traces is 25 mils, this includes adjacent signal layers.
>> Memory address, data, and control lines must be routed as separate groups and treated as different signal types.
>> The MD, DQM, CS#, CKE, SRAS#, SCAS#, WE#, and MA signals (between BX and SODIMM) must be between 1" and 3" in length, matched to within 600 mils.

Memory Bus GROUPS -- SODIMM Names

>> Address Signals: MAA[13:0]
>> Data Signals: MD#[63:0]
>> Control Signals:

CKE[1:0], SMBDATA, SMBCLK, CSA[1:0]#, WE_A#, SCAS_A#, SRAS_A#

PCI Bus Specific Routing Requirements

>> The 440MX must be the last device on the PCI bus.
>> PCI bus max length must be less than 6".

PCI Bus GROUPS

>> Address/Data Signals: AD[31:0]
>> Control Signals:

BUSMD1#, C/BE[3:0]#, REQ1#, GNT1#, INT[A:D]#, PCIRST#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PERR#, PAR, LOCK#

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Title: Routing Guidelines
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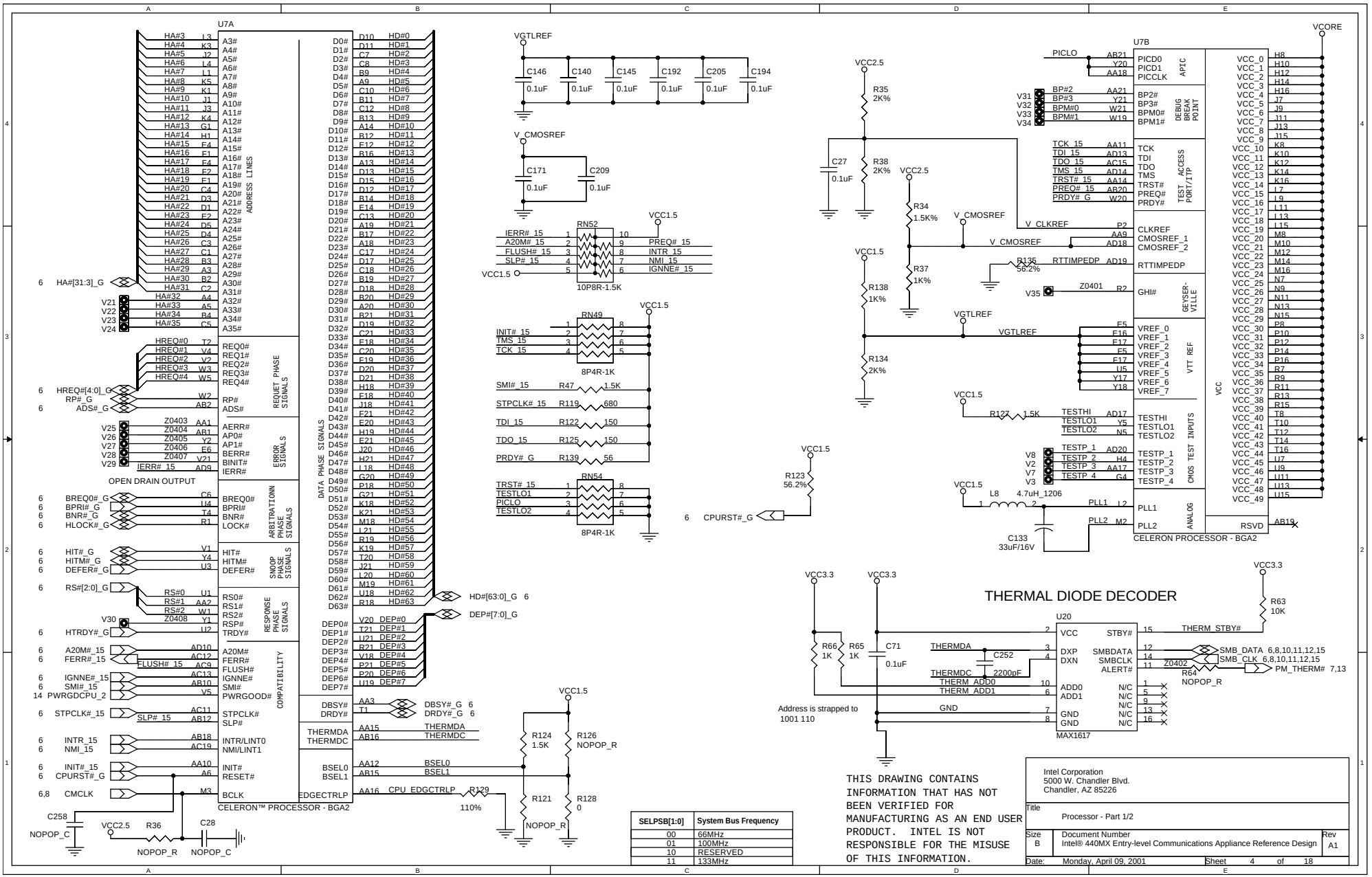
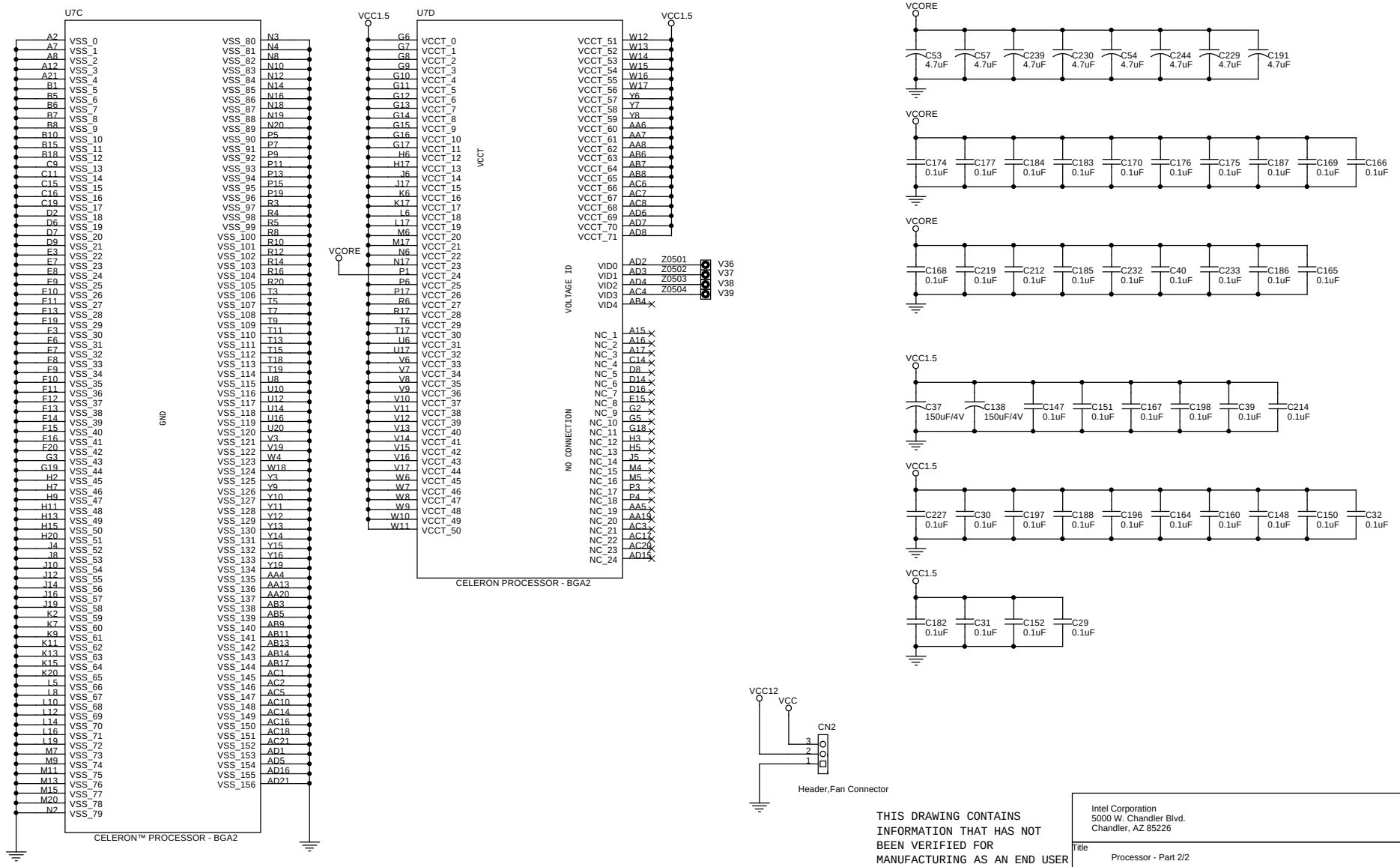


SELPSB[1:0]	System Bus Frequency
00	66MHz
01	100MHz
10	RESERVED
11	133MHz



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Title: Processor - Part 2/2

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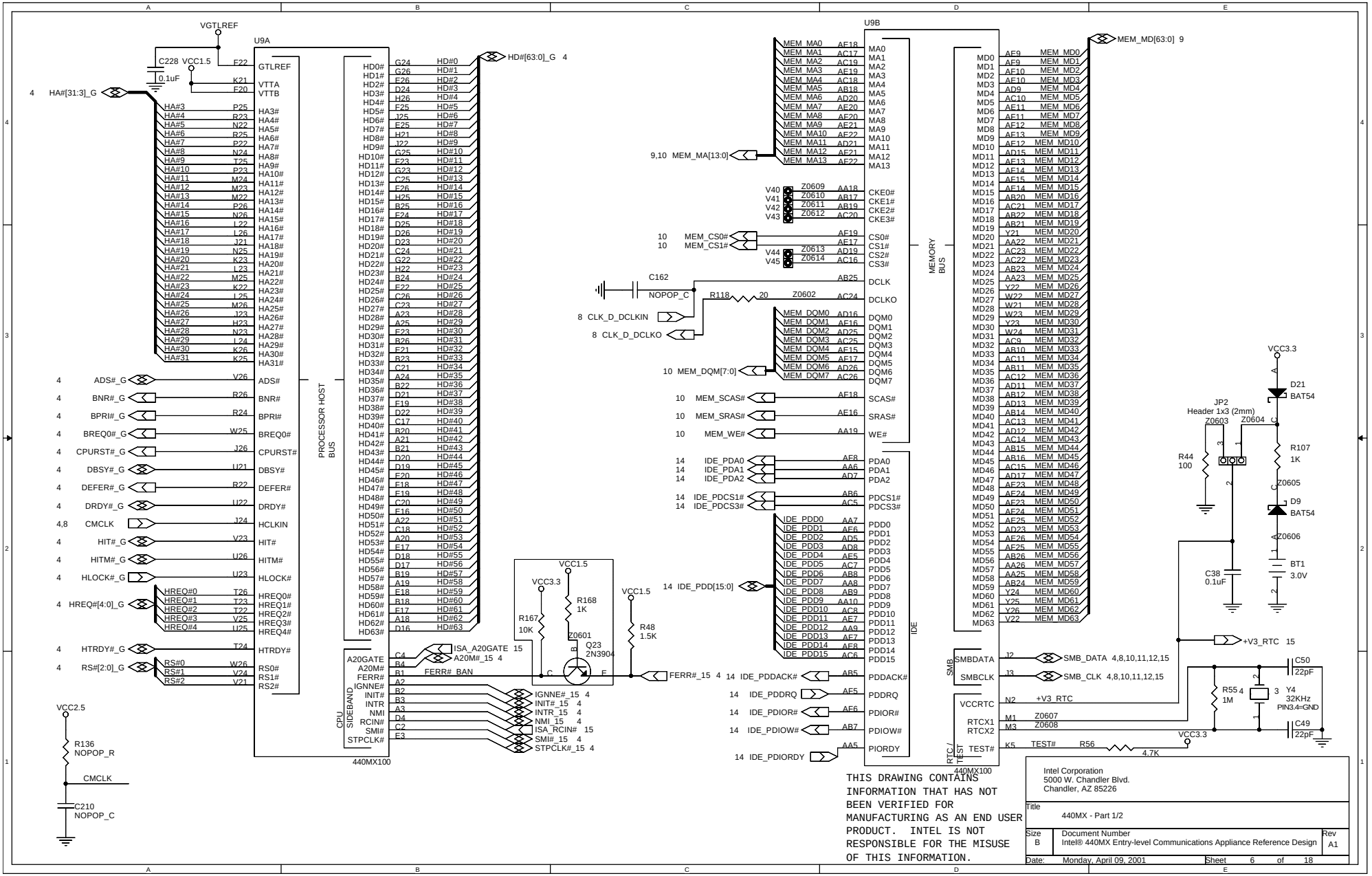
U9A
U9B
VGTLREF
C228 0.1uF
VCC1.5
GTLREF
VTTA
VTTB
HA#[31:3]_G
PROCESSOR HOST BUS
HD#[63:0]_G
ADS#_G
BNR#_G
BPRI#_G
BREQ0#_G
CPURST#_G
DBSY#_G
DEFER#_G
DRDY#_G
CMCLK
HIT#_G
HITM#_G
HLOCK#_G
HREQ#[4:0]_G
HTRDY#_G
RS#[2:0]_G
CPU SIDEBAND
A20GATE
A20M#
FERR#
IGNNE#
INIT#
INTR
NMI
RCIN#
SMI#
STPCLK#
ISA_A20GATE
A20M#_15
FERR# BAN
IGNNE#_15
INIT#_15
INTR_15
NMI_15
ISA_RCIN#
SMI#_15
STPCLK#_15
440MX100
VCC3.3
R168 1K
R167 10K
Z0601
Q23 2N3904
R48 1.5K
FERR#_15
VCC2.5
R136 NOPOP_R
C210 NOPOP_C
MEMORY BUS
MEM_MA[13:0]
CKE0#
CKE1#
CKE2#
CKE3#
MEM_CS0#
MEM_CS1#
C162 NOPOP_C
R118 20
Z0602
DCLK
DCLKO
CLK_D_DCLKIN
CLK_D_DCLKO
MEM_DQM[7:0]
SCAS#
SRAS#
WE#
IDE
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDD[15:0]
IDE_PDDACK#
IDE_PDDRQ
IDE_PDIOR#
IDE_PDIOW#
IDE_PDIORDY
MEM_MD[63:0]
SMB
SMBDATA
SMBCLK
SMB_DATA
SMB_CLK
VCCRTC
RTCX1
RTCX2
RTC / TEST
TEST#
R56 4.7K
+V3_RTC
JP2 Header 1x3 (2mm)
Z0603
Z0604
R44 100
R107 1K
Z0605
Z0606
D21 BAT54
D9 BAT54
BT1 3.0V
C38 0.1uF
C50 22pF
C49 22pF
R55 1M
Y4 32KHz
PIN3.4=GND
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Title
440MX - Part 1/2
Size B
Document Number
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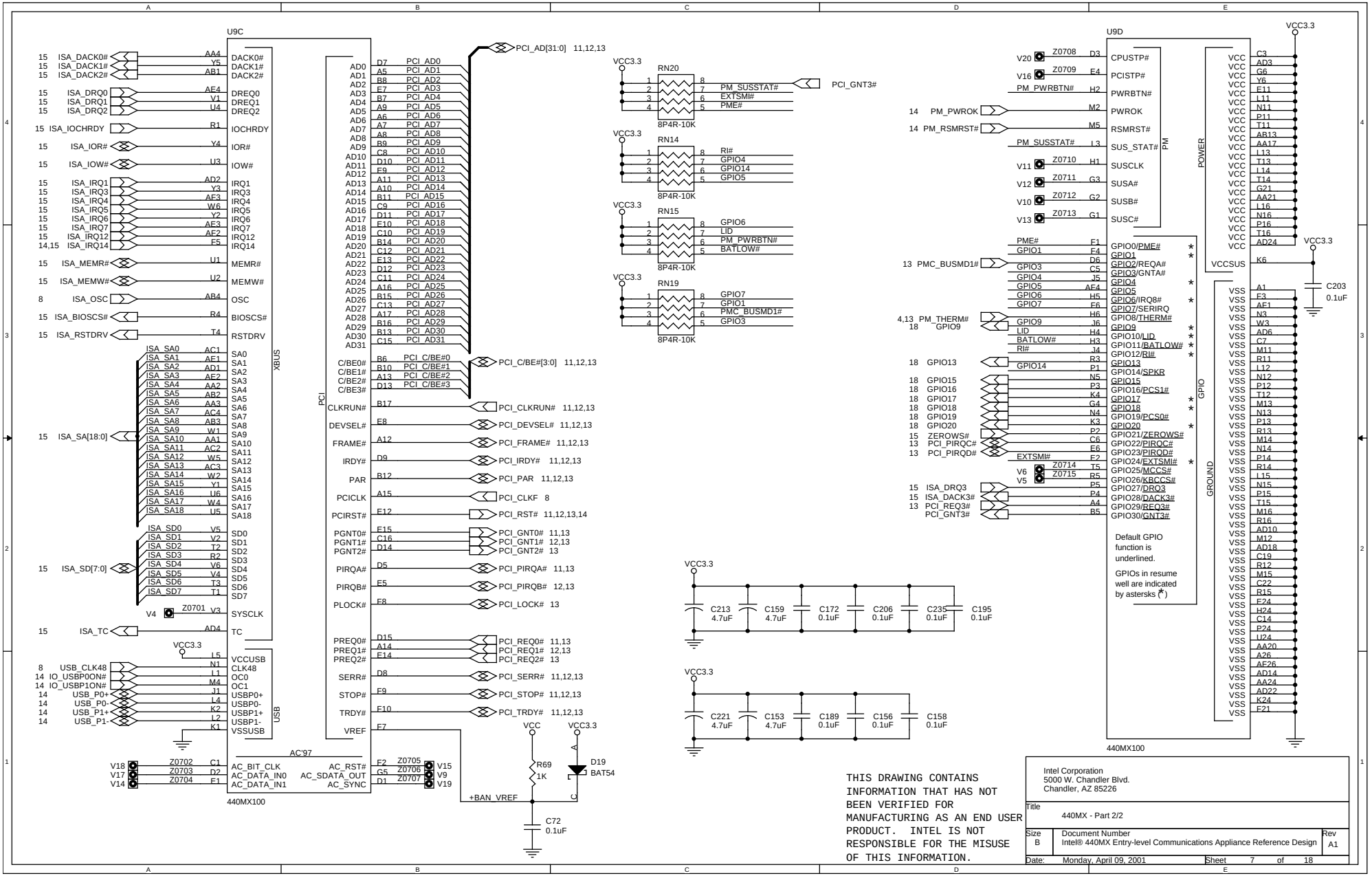
U9C
440MX100
XBUS
PCI
USB
AC'97
U9D
PM
POWER
GPIO
GROUND
Default GPIO function is underlined.
GPIOs in resume well are indicated by asterisks (*)
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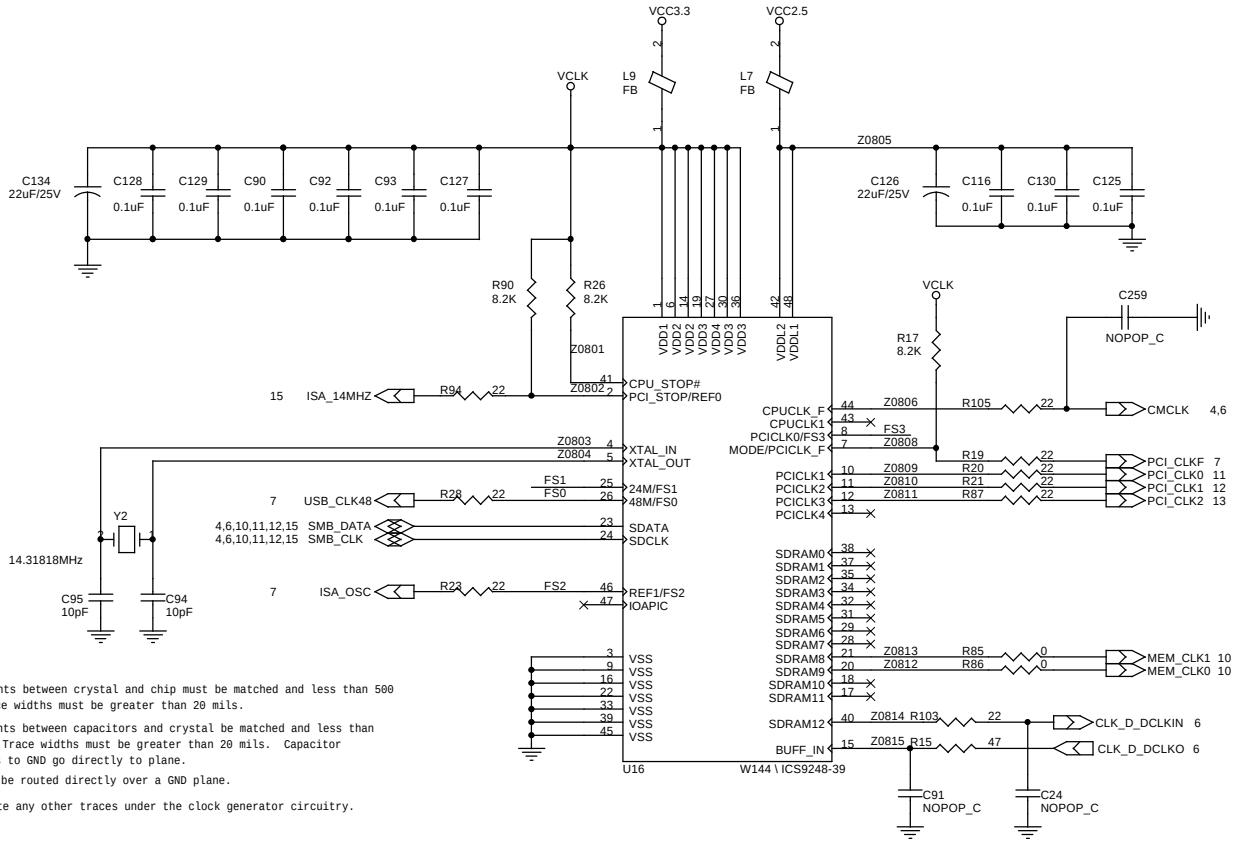
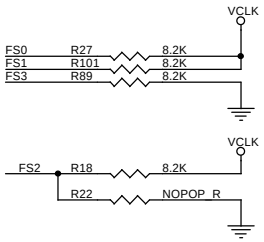


>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.

>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.

>> Trace must be routed directly over a GND plane.

>> Do not route any other traces under the clock generator circuitry.



FS2	FS1	FS0	
0	1	1	66MHz
1	1	1	100MHz

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Title: Clocking

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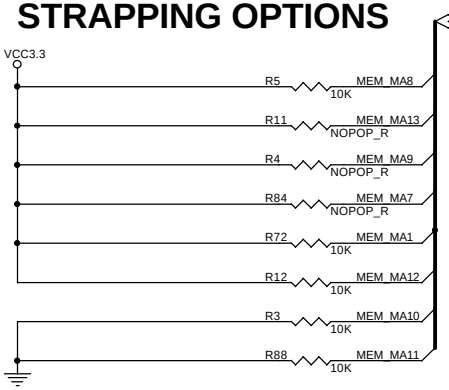
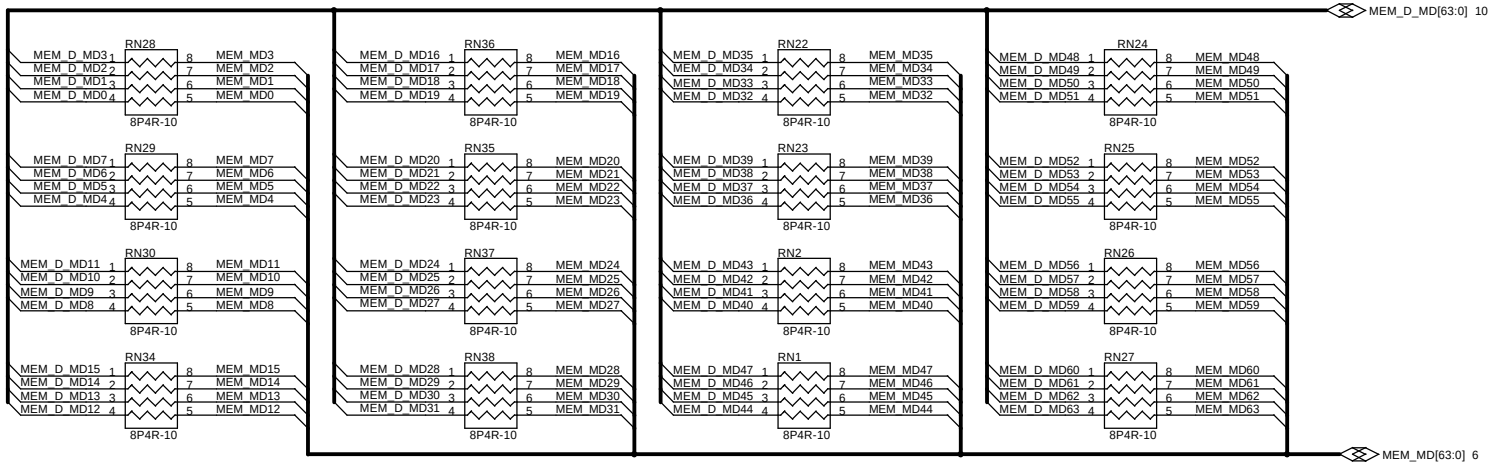
STRAPPING OPTIONS

BUS RATIO SETTINGS				
NMI (MA13)	INTR (MA9)	IGNNE# (MA7)	A20M# (MA1)	CPU Frequency
Lo	Lo	Hi	Lo	300MHz (3/1)
Lo	Hi	Hi	Lo	350MHz (7/2)
Lo	Lo	Lo	Hi	400MHz (4/2)
Lo	Hi	Lo	Hi	450MHz (9/2)
Lo	Lo	Hi	Hi	500MHz (5/1)
Lo	Hi	Hi	Hi	550MHz (11/2)
Hi	Lo	Lo	Lo	600MHz (6/1)
Hi	Hi	Lo	Lo	650MHz (13/2)
Hi	Lo	Hi	Lo	700MHz (7/1)
Hi	Hi	Hi	Lo	750MHz (15/2)
Hi	Lo	Lo	Hi	800MHz (8/1)



	LINE	FUNCTION	PULL-UP	PULL-DOWN	440MX100 DEFAULT
*	MA8	High Frequency VCO	High Speed	Normal Speed	Pull down
	MA13	CPU Clock Ratio (NMI)	Not used		Pull down
	MA9	CPU Clock Ratio (INTR)			Pull down
	MA7	CPU Clock Ratio (IGNNE#)			Pull down
	MA1	CPU Clock Ratio (A20M#)			Pull down
	MA12	Host Frequency Select	100MHz	66MHz	Pull down
*	MA10	Quick Start Select	Quick Start		Pull up
*	MA11	Pipelined Operation	Pipelined	Non-pipelined	Pull up



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Title: Memory Data Bus Damping Resistors

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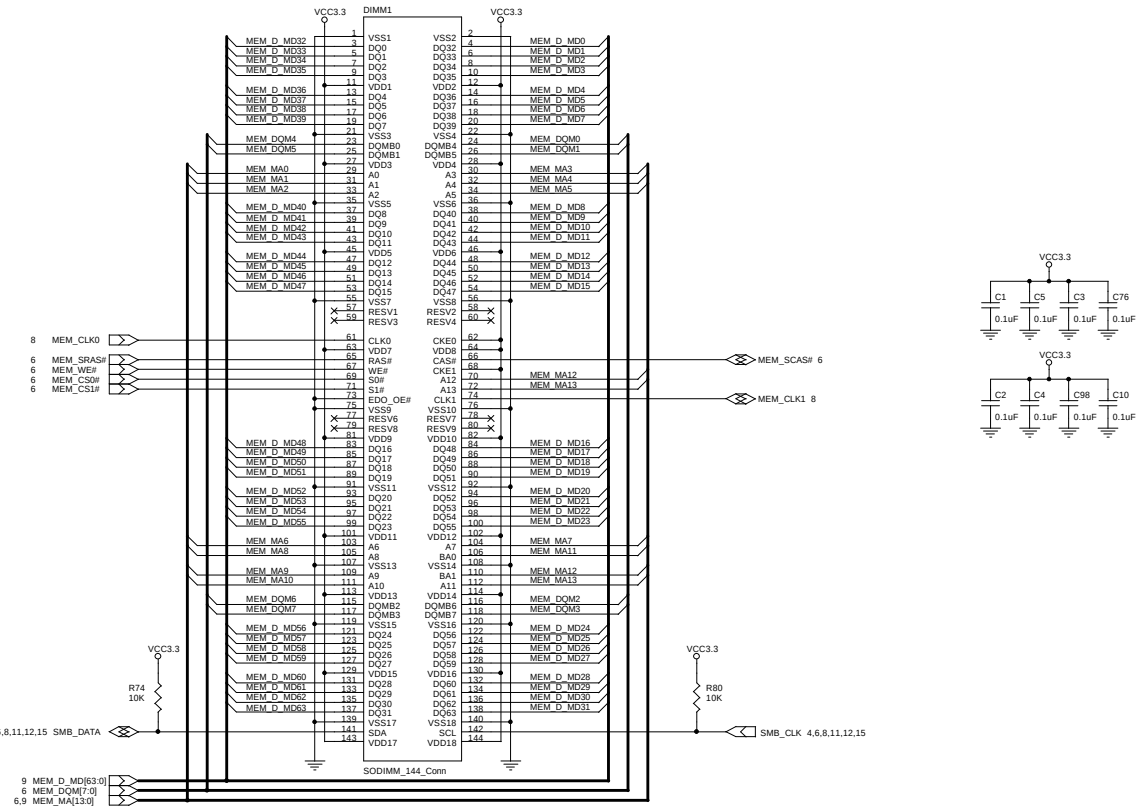

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Title: SO-DIMM Connector

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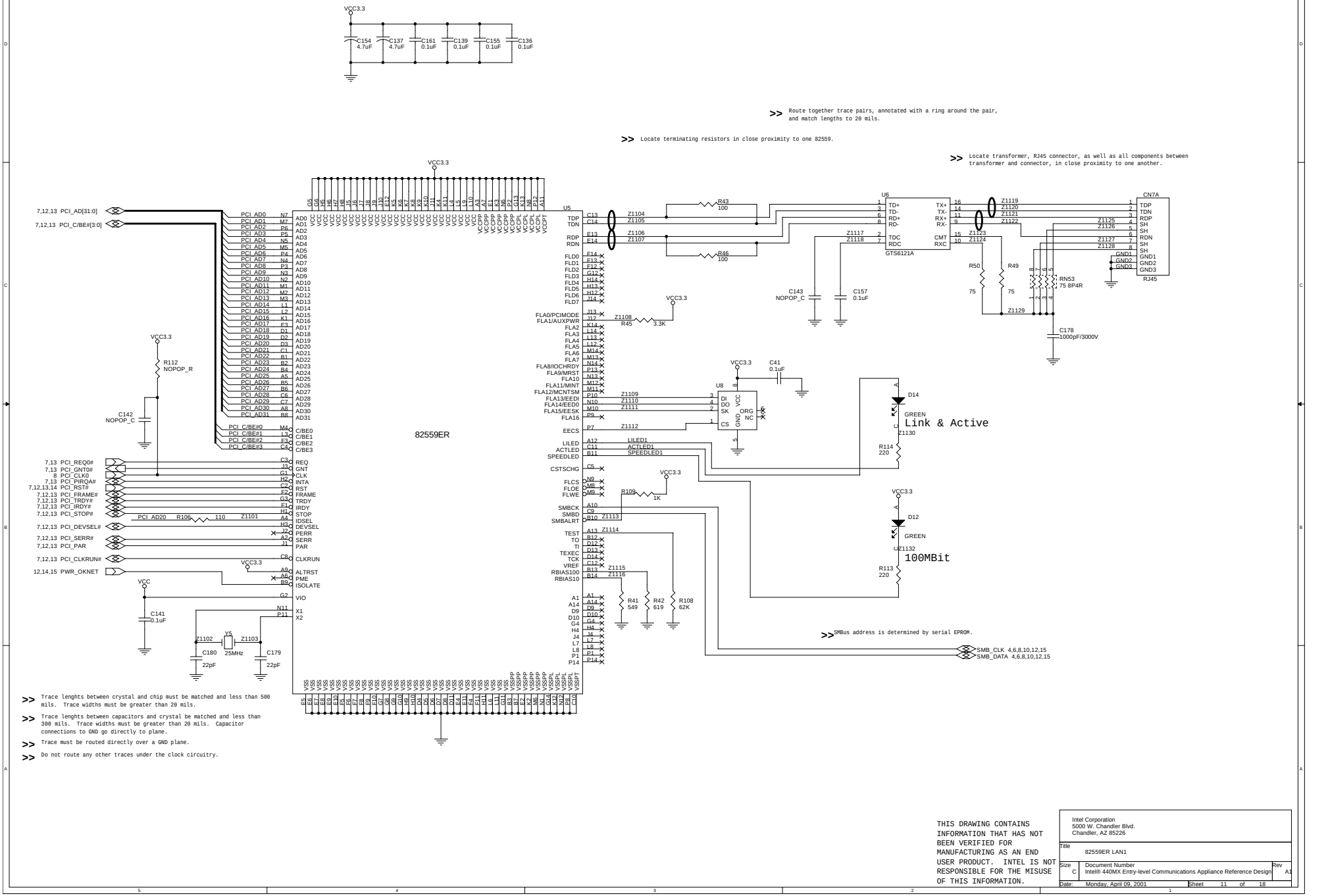
VCC3.3
C154 4.7uF
C137 4.7uF
C161 0.1uF
C139 0.1uF
C155 0.1uF
C136 0.1uF
>> Route together trace pairs, and match lengths to 20 mils.
>> Locate terminating resistors in close proximity to one 82559.
>> Locate transformer, RJ45 connector, as well as all components between transformer and connector, in close proximity to one another.
82559ER
U5
U6
GTS6121A
CN7A
RJ45
U8
R112 NOPOP_R
C142 NOPOP_C
C143 NOPOP_C
C157 0.1uF
C141 0.1uF
C180 22pF
C179 22pF
Y5 25MHz
Z1102
Z1103
R43 100
R46 100
R45 3.3K
R109 1K
R41 549
R42 619
R108 62K
R114 220
R113 220
R50 75
R49 75
RN53 75 8P4R
C178 1000pF/3000V
C41 0.1uF
D14
GREEN
Link & Active
Z1130
D12
GREEN
Z1132
100MBit
R106 110 Z1101
PCI_AD20
>> SMBus address is determined by serial EPROM.
SMB_CLK 4,6,8,10,12,15
SMB_DATA 4,6,8,10,12,15
>> Trace lenghts between crystal and chip must be matched and less than 500 mils. Trace widths must be greater than 20 mils.
>> Trace lenghts between capacitors and crystal be matched and less than 300 mils. Trace widths must be greater than 20 mils. Capacitor connections to GND go directly to plane.
>> Trace must be routed directly over a GND plane.
>> Do not route any other traces under the clock circuitry.
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Title
82559ER LAN1
Size C
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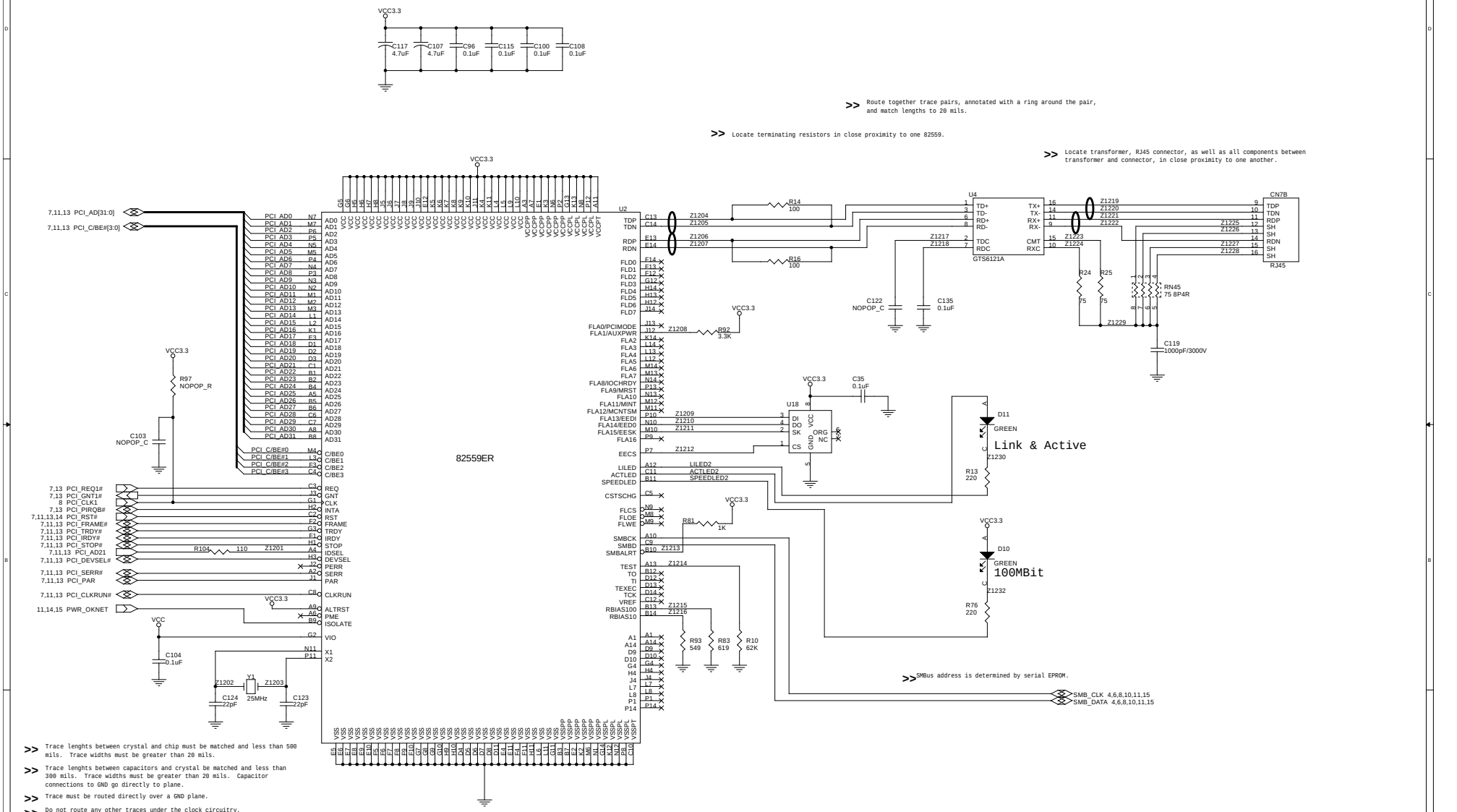

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Title	82559ER LAN2
Size	C
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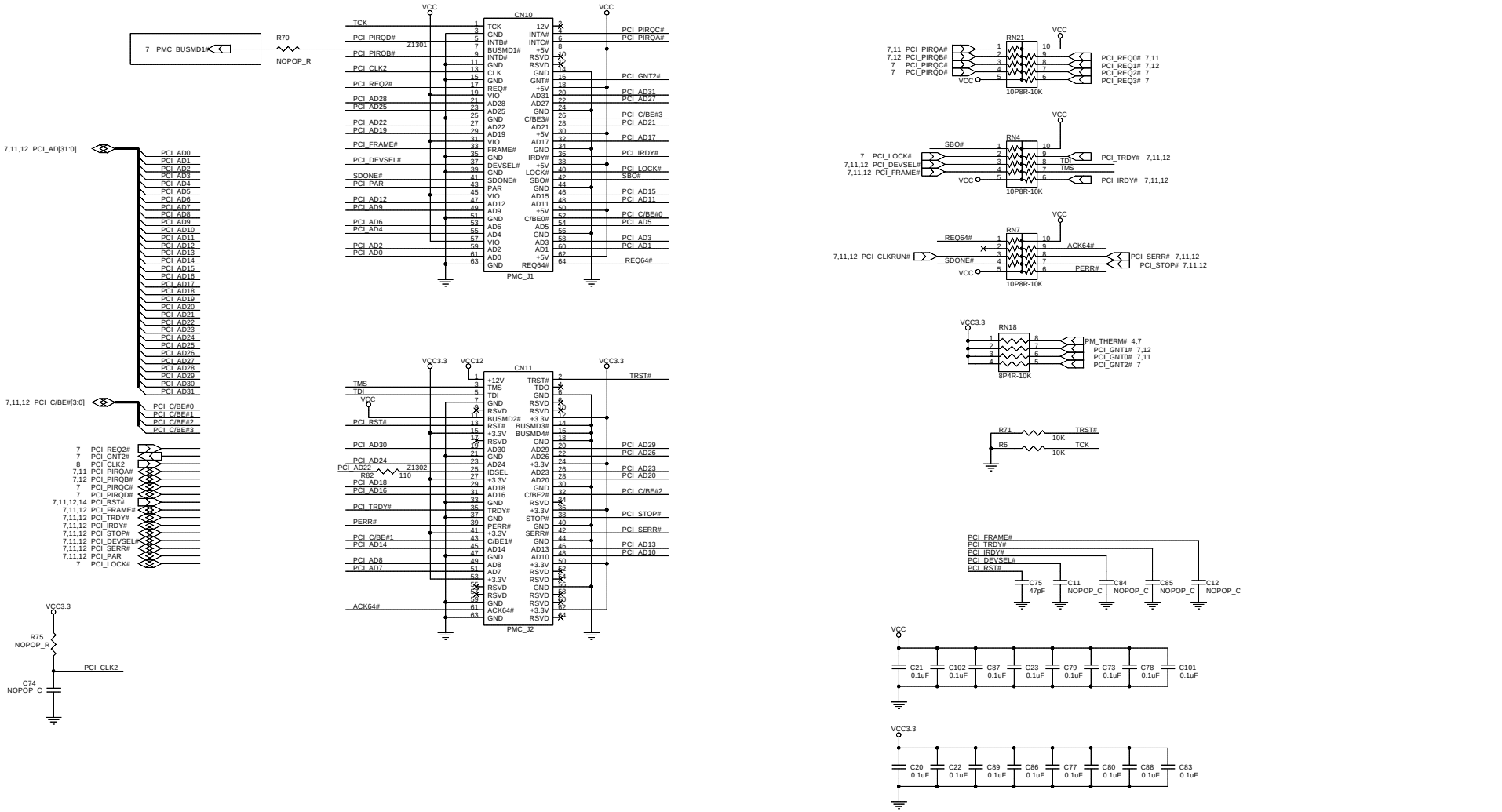

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Title	PMC Connector	
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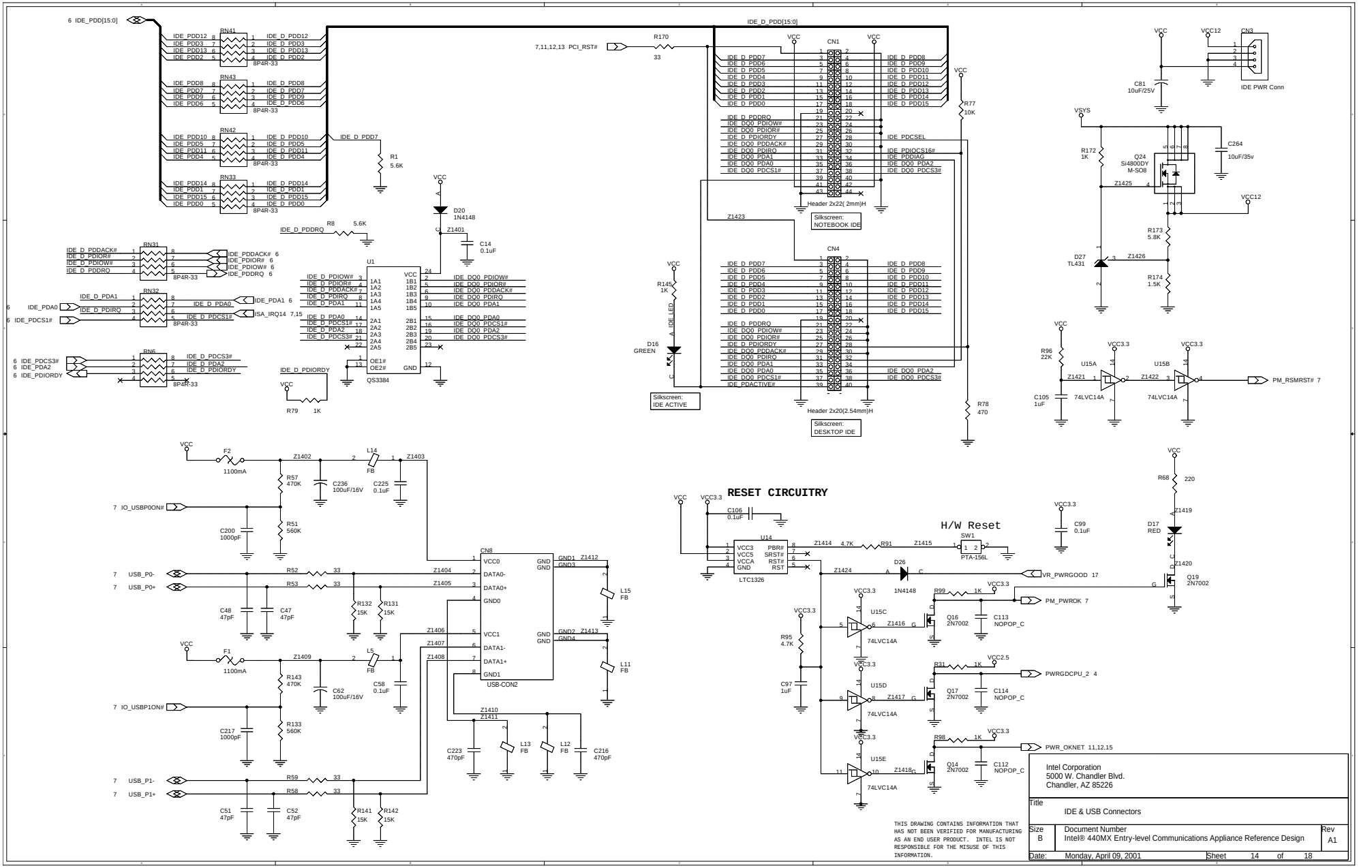
RESET CIRCUITRY
H/W Reset
USB-CON2
LTC1326
Silkscreen: NOTEBOOK IDE
Silkscreen: IDE ACTIVE
Silkscreen: DESKTOP IDE
IDE PWR Conn
Header 2x22(2mm)H
Header 2x20(2.54mm)H
QS3384
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IDE & USB Connectors
Size B
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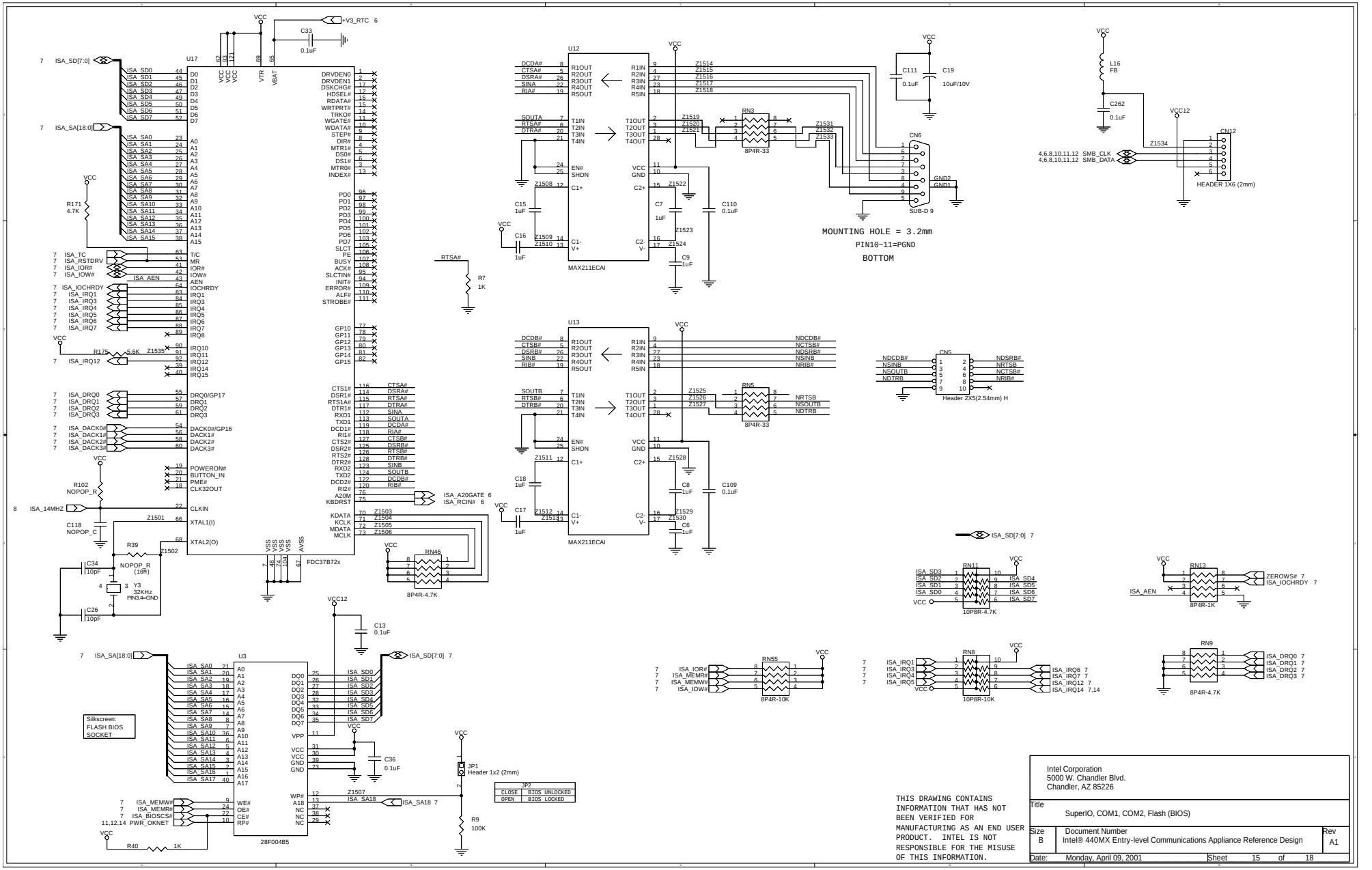
U17
FDC37B72x
U12
MAX211ECAI
U13
MAX211ECAI
U3
28F004B5
MOUNTING HOLE = 3.2mm
PIN10~11=PGND
BOTTOM
Silkscreen:
FLASH BIOS
SOCKET
JP2
CLOSE | BIOS_UNLOCKED
OPEN | BIOS_LOCKED
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Title
SuperIO, COM1, COM2, Flash (BIOS)
Size B
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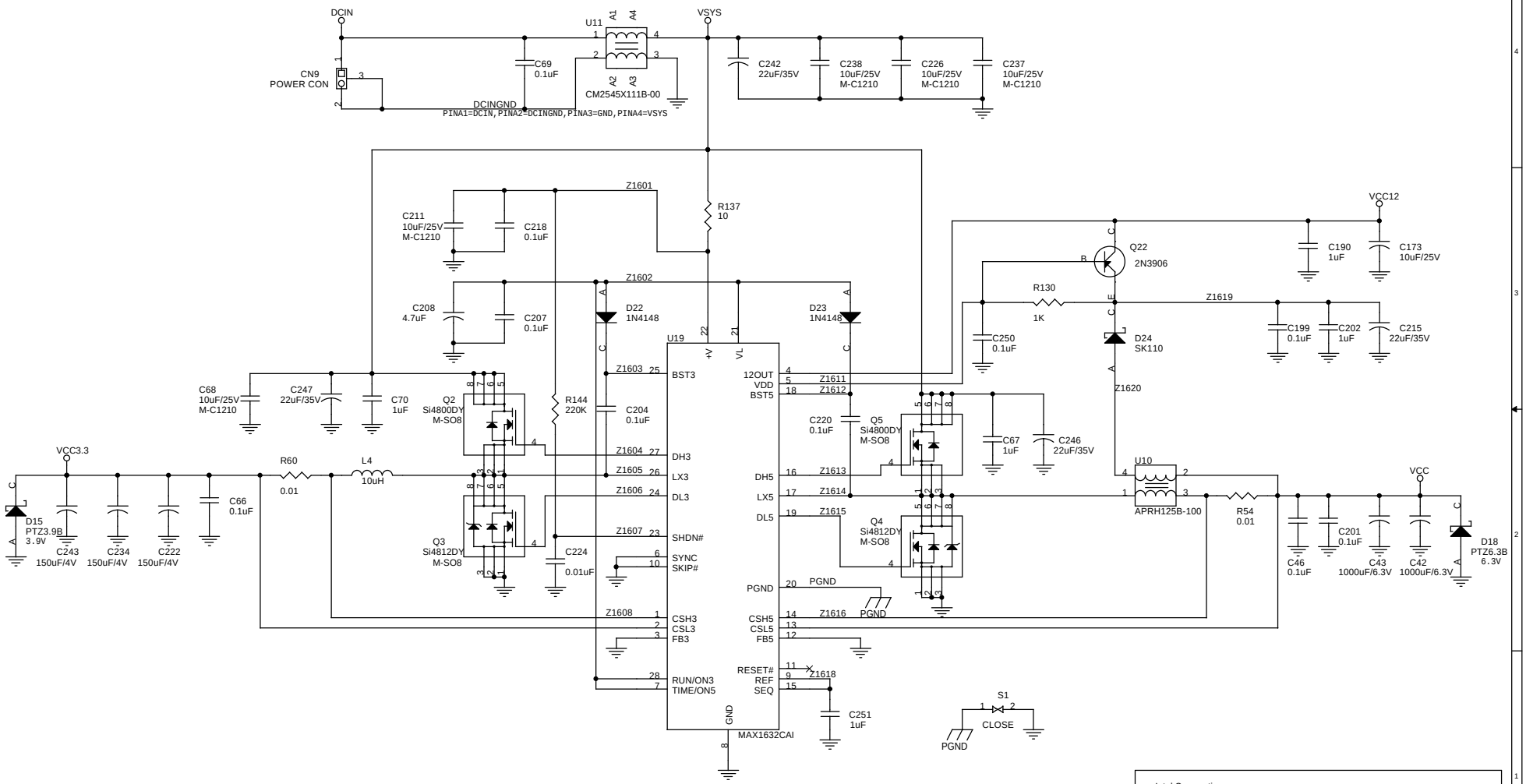

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Title: Voltage Regulator - Part 1/2

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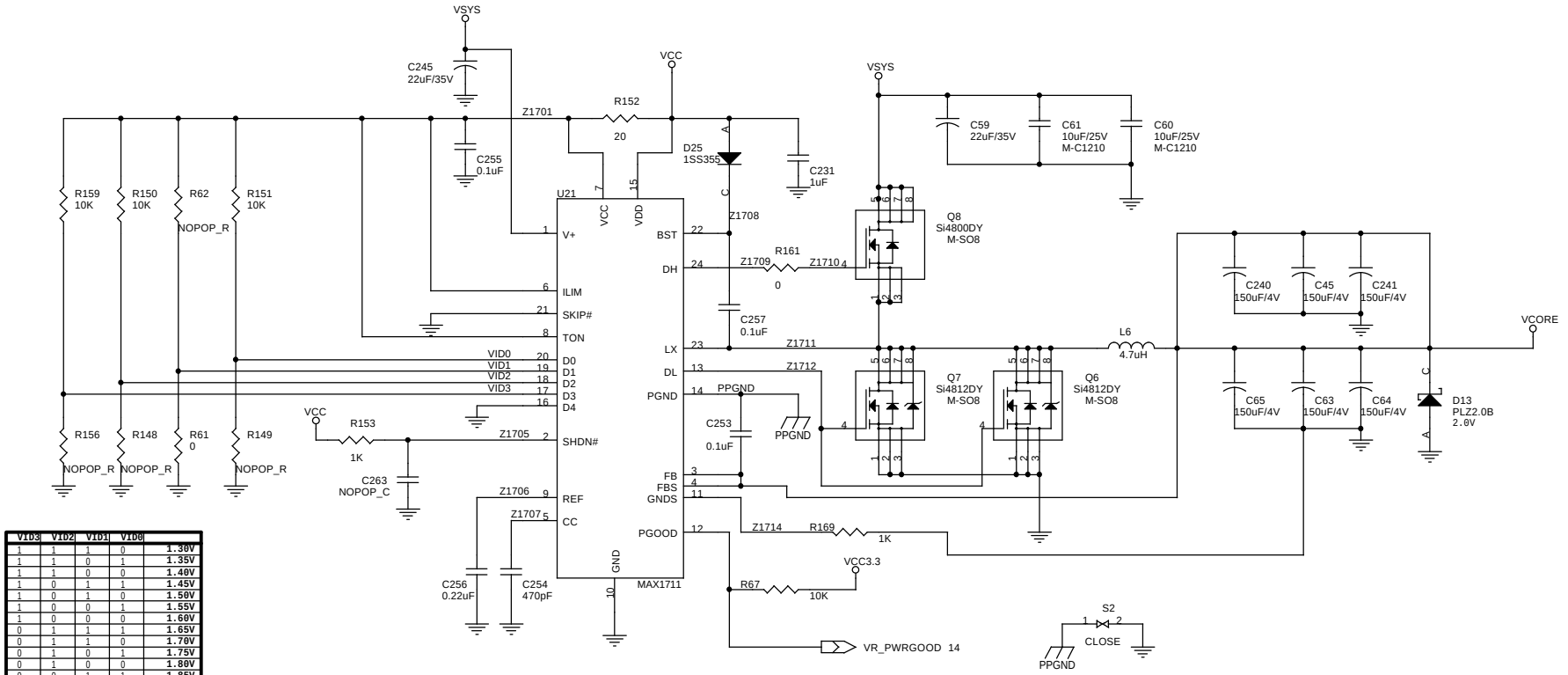
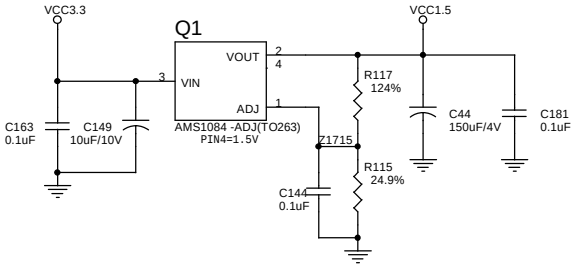
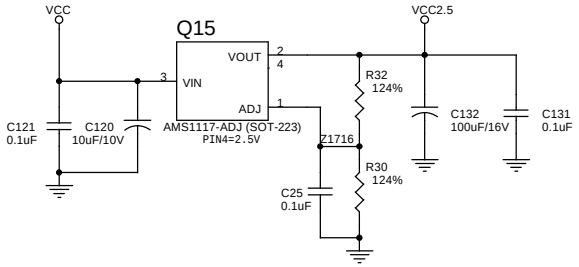


VID3	VID2	VID1	VID0	
1	1	1	0	**1.30V**
1	1	0	1	**1.35V**
1	1	0	0	**1.40V**
1	0	1	1	**1.45V**
1	0	1	0	**1.50V**
1	0	0	1	**1.55V**
1	0	0	0	**1.60V**
0	1	1	1	**1.65V**
0	1	1	0	**1.70V**
0	1	0	1	**1.75V**
0	1	0	0	**1.80V**
0	0	1	1	**1.85V**
0	0	1	0	**1.90V**
0	0	0	1	**1.95V**
0	0	0	0	**2.00V**





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Title: Voltage Regulator - Part 2/2

Size: B | Document Number: Intel® 440MX Entry-level Communications Appliance Reference Design | Rev: A1

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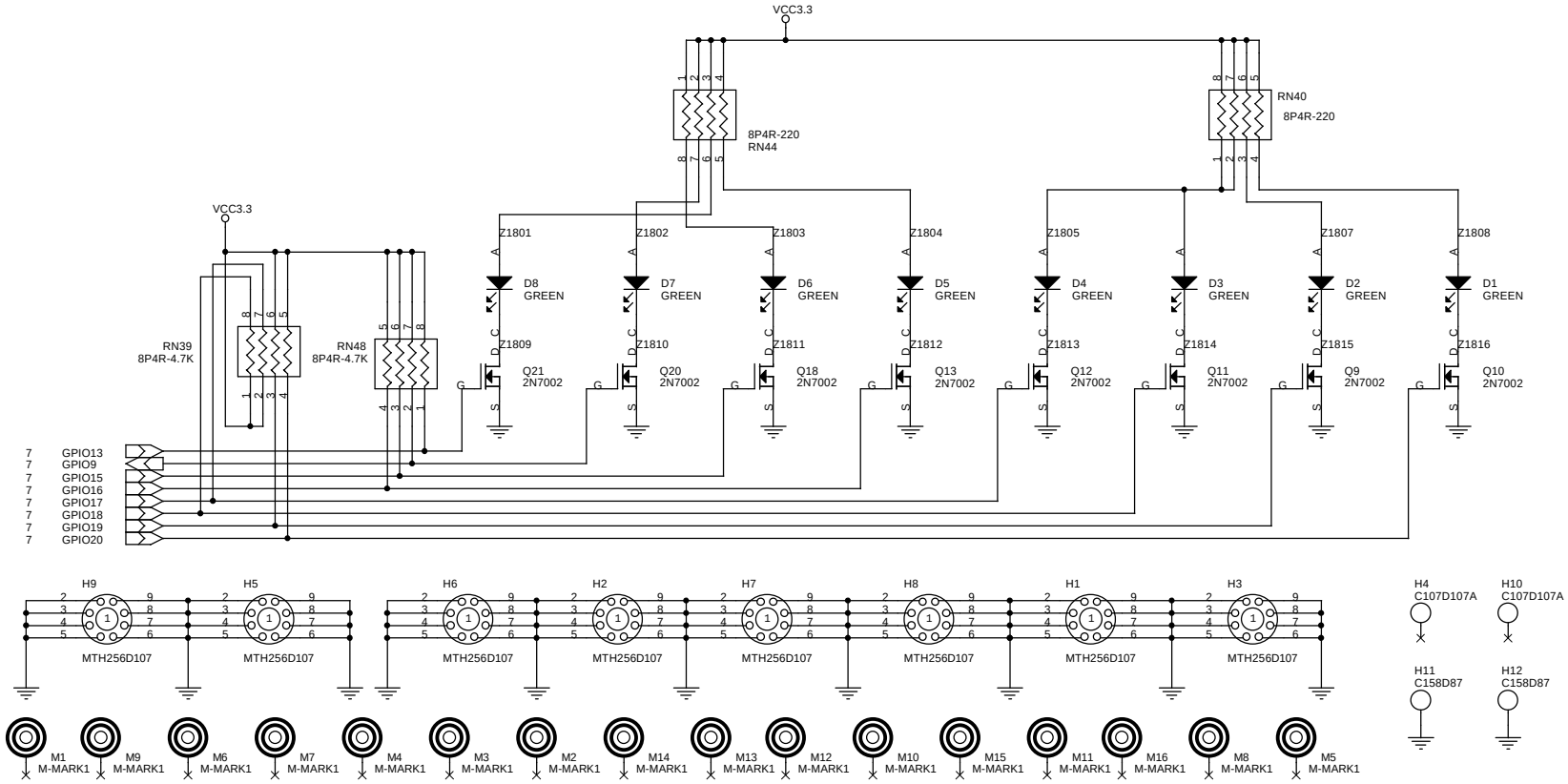

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Title	GPIO LEDs	
Size B	Document Number: Intel® 440MX Entry-level Communications Appliance Reference Design	Rev A1
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